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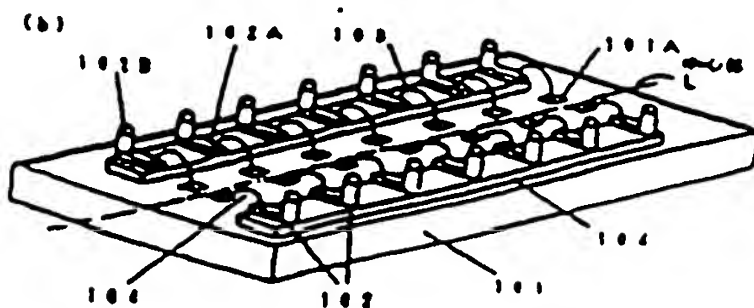
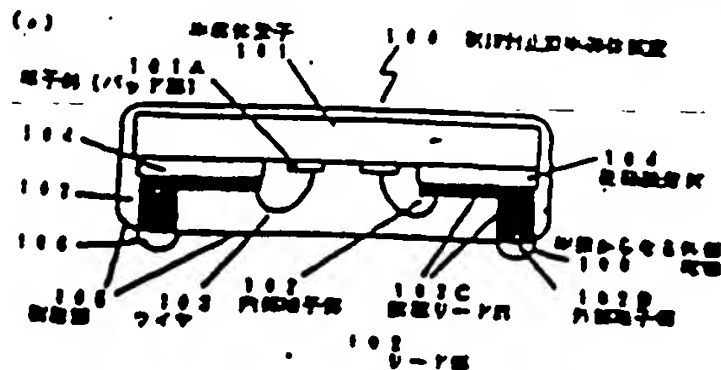
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(54) 【発明の名称】 積層型半導体装置とそれに用いられるリードフレーム、及び積層型半導体装置の製造方法

(57) 【要約】

【目的】 更なる積層型半導体装置の高集積化、高信頼化が求められている中、半導体装置パッケージサイズにおけるチップの占有率を上げ、半導体装置の小型化に対応させ、同時に従来の T S O P 等の小型パッケージに懸念であった更なる多ピン化を実現した積層型半導体装置を提供する。

【構成】 半導体装置の端子側の面に、半導体装置の端子と電気的に接続するための内部端子部と、半導体装置の端子側の面へ配設して外部へと向く外部端子部への接続のための外部端子部と、前記内部端子部と外部端子部とを連結する接続リード部とを一体とした積層のリード部とを、絶縁性材料層を介して、積層して設けてあり、且つ、前記基板への実装のための半導体からなる外部電極を前記積層の各リードの外部端子部に連結させ、少なくとも前記半導体からなる外部電極の一部は前記部より外部に露出させて設けている。



【請求項4】半導体素子の端子側の面に、半導体素子と電気的に接続するための内部端子部と、半導体素子の端子側の面へ直交して外部へと向く外部回路への接続のための外部端子部と、前記内部端子部と外部端子部とを連絡するはね状リード部とを一体とした装置のリード部とを、はね状部材層を介して、固定して設けてお、且つ、前記基板層への実装のための半田からなる外電極を前記装置の各リードの外側端子部に連絡させ、なくとも前記半田からなる外側電極の一部は前記部と外部に露出させて設けている前記封止型半導体装置の他方法であつて、少なくとも、(A)エッチング加工で、半導体素子の端子と電気的に接続するための内部端子部と、外部回路と接続するための外部端子部と、前記内部端子部と外部端子部とを連絡するはね状リード部とを一体とし、該外部端子部を、はね状リード部を介して、リードフレーム部から直交する一方方向に突出させ、前記先端部同士で連絡部を介して接続する一方の内部端子部を露出させており、且つ、各外部端子部の外側で、リード部と連絡し、一体として全体を保持する外に設けているリードフレームを作製する工程、(B)リードフレームの外側端子部側でない面(裏面)に材料を設け、打ち抜き金型により、前記する内部端子部を接続する連絡部とは連絡部に対応する位置に設

(D) 本選は素子の電子銃と、切斷されて、その先端へ形成された内腔電子銃の先端部とをワイヤボンディングした後に、摩擦により内腔電子銃座のみを本座に取出させて今後は封止する工程、(E) 前記前記に取出した内腔電子銃座に本座からなる外腔電極を形成する工程、とを含むことを特徴とする摩擦封止型本選装置の製造方法。

【事業上の計画方針】本見解は、年産低炭素を達成する
徹底削減型の年産低炭素（プラスティックパッケージ）に
関し、特に、コスト削減を向上させ、より、多岐にわた
る年産低炭素とその削減方法に及ぼす。

(0 0 0 2)

10 (従来の技術) 近年、半導体装置は、高集積化、小型化技術の進歩と電子回路の高性能化と経済的小型化の傾向(時代)から、LSIのASICに代替されるように、ますます高集積化、高機能化になってきている。これに伴い、リードフレームを用いた封止型の半導体装置ブラスタックパッケージにおいても、その集積のトレンドが、SOJ (Small Outline)-Lead Package) や QFP (Quad Flat Package) のような表面実装型のパッケージを経て、TSOP (Thin Small Outline Package) の集積による薄型化を主眼としたパッケージの小型化へ、さらにはパッケージ内部の3次元化によるチップ収容効率向上を目的としたLOC (Lead On Chip) の集積へと進展して来た。しかし、表面封止型半導体装置パッケージには、高集積化、高機能化とともに、更に一層の多ピン化、薄型化、小型化が求められており、上記従来のパッケージにおいてもチップ外周部分のリードの引き出しがあるため、パッケージの小型化に限界が見えて来た。また、TSOP等の小型パッケージにおいては、リードの引き出し、ピンピッチから多ピン化に対しても限界が見えて来た。

(0 0 0 3)

〔説明が加えようとする課題〕上記のように、更なる
回路封止型半導体装置の高集積化、多機能化が求めら
れており、回路封止型半導体装置パッケージの層の多ビ
ン化、薄型化、小型化が求められている。本説明は、こ
のような状況のもと、半導体装置パッケージサイズにお
けるチップの占有率を上げ、半導体装置の小型化に対応
させ、回路基板への実装面積を低減せよ、即ち、回路
基板への実装密度を向上させることができる回路封止型
半導体装置を提供しようとするものである。また、回路

に従来のT S O P 系の小型パッケージに搭載であった更なる多ピン化を実現しようとするものである。

(0 0 0 4)

(注釈を省略するための手段) 本発明の積層型半導体装置は、半導体素子の端子側の面に、半導体素子の端子と電気的に接続するための内部端子部と、半導体素子の端子側の面へ突き出て外部へと向く外部端子部への接続のための外部端子部と、前記内部端子部と外部端子部とを接続する接続リード部とを一体とした複数のリード部とを、絶縁性層を介して、露出して設けており、且つ、図 1 及び図 2 への矢印の方向に半導体素子からなる外部端子部を前記複数のリード部の外部端子部に露出させ、少なくとも前記半導体素子からなる外部端子部の一部は前記露出より外部へ突出させて設けていることを特徴とするものである。尚、上記において、内部端子部と外部端子部とを一体とした複数のリード部の配列を半導体素子の端子側面に二次元的に配列し、外部端子部を半導体素子の端子側面に二次元的に配列し、外部端子部を半導体素子の端子側面に二次元的に配列することにより B C A (B o i l C r i d A r i o y) タイプの積層型半導体装置とすることとする。

(0 0 0 5) そして、上記において、半導体素子の端子は半導体素子の端子側の面の一列の辺の中心部上に設けて設けられており、リード部は複数の端子を挟むように対向し前記一列の辺に沿って設けられていることを特徴とするものである。また、本発明のリードフレームは、積層型半導体装置のリードフレームであって、半導体素子の端子と電気的に接続するための内部端子部と、外部端子部とを接続するための外部端子部と、前記内部端子部と外部端子部とを接続する接続リード部とを一体とし、該外部端子部を、接続リード部を介して、リードフレーム面から突出する一方向側に突出させ、対向し先端部同士で接続部を介して接続する一列の内部端子部を露出させており、且つ、各外部端子部の外側で、接続リード部と接続し、一体として全体を保持する外側部を設けていることを特徴とするものである。尚、上記リードフレームにおいて、内部端子部と外部端子部とをそれぞれを接続する接続リード部とを一体とした複数のリード部をリードフレーム面に二次元的に配列するとして形成することにより B C A (B o i l C r i d A r i o y) タイプの積層型半導体装置のリードフレームとすることとする。

(0 0 0 6) 本発明の積層型半導体装置の製造方法は、半導体素子の端子側の面に、半導体素子の端子と電気的に接続するための内部端子部と、半導体素子の端子側の面へ突き出て外部へと向く外部端子部への接続のための外部端子部と、前記内部端子部と外部端子部とを接続する接続リード部とを一体とした複数のリード部とを、絶縁性層を介して、露出して設けており、且つ、図 1 及び図 2 への矢印の方向に半導体素子からなる外部端子部を前記複数のリード部の外部端子部に露出させ、少なくとも前記半導体素子からなる外部端子部の一部は前記露出より外部へ突出させて設けていることを特徴とするものである。

図 1 及び図 2 への矢印の方向に半導体素子からなる外部端子部を前記複数のリード部の外部端子部に露出させ、少なくとも前記半導体素子からなる外部端子部の一部は前記露出より外部へ突出させて設けていることを特徴とするものである。尚、上記において、内部端子部と外部端子部とを一体とした複数のリード部の配列を半導体素子の端子側面に二次元的に配列し、外部端子部を半導体素子の端子側面に二次元的に配列することにより B C A (B o i l C r i d A r i o y) タイプの積層型半導体装置とすることとする。

10 (0 0 0 7) (作用) 本発明の積層型半導体装置は、上記のような構成にすることにより、半導体装置パッケージサイズにおけるチップの占有率を上げ、半導体装置の小型化に対応できるものとしている。即ち、半導体装置の図 1 及び図 2 への矢印の方向に半導体素子からなる外部端子部を前記複数のリード部の外部端子部に露出させ、少なくとも前記半導体素子からなる外部端子部の一部は前記露出より外部へ突出させて設けていることを特徴とするものである。尚、上記において、内部端子部と外部端子部とを一体とした複数のリード部の配列を半導体素子の端子側面に二次元的に配列し、外部端子部を半導体素子の端子側面に二次元的に配列することにより B C A (B o i l C r i d A r i o y) タイプの積層型半導体装置とすることとする。

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とがてら、本発明の製造方法及び装置の構成は、上記リードフレームを用いて、リードフレームの外周部を形成しない面（底面）に絶縁材を形成し、第1層を金箔により、方向する内部端子部を形成する導電層と導電層に形成する位置に形成された絶縁材とを形成し、リードフレームの形成された部分が半導体素子の端子部にくるようにして、絶縁層を介して、リードフレーム全体を半導体素子へ搭載し、リードフレームの外周部を含む半導体素子の部分を形成し、金箔により形成することにより、内部端子と外部端子を一体とした構造を多ピン構造上に形成した。本発明の、半導体素子の小型化が可能で、且つ、多ピン化が可能で、製造方法及び装置の構成を可能としている。

(0 0 0 8)

(実施例) 本発明の製造方法及び装置の構成を以下、図にそって説明する。図 1 (a) は本発明の製造方法及び装置の断面図であり、図 1 (b) は本発明の平面図である。図 1 中、100は製造方法及び装置、101は半導体素子、102はリード部、102Aは内部端子部、102Bは外部端子部、102Cは形成リード部、101Aは端子部（パッド部）、103はワイヤ、104は絶縁層、105は導電層、106は半田（ペースト）からなる外部電極である。本発明の製造方法及び装置は、形成するリードフレームを用いたもので、内部端子部102A、外部端子部102Bを一体とした半導体のリード部102を多ピン構造素子101上に絶縁層104を介して形成し、且つ、外部端子部102B先に半田からなる外部電極を形成部105より外部へ突出させて設けた。パッケージ構造が半導体素子の面側に形成する製造方法及び装置であり、図1(a)に示すように、半田ペースト106を形成し、図1(b)に示すように、半導体素子101の端子部（パッド部）101Aは半導体素子の中心部101を中心として2層づつ、中心部101に形成され、リード部102は、内部端子部102Aが形成端子部（パッド部）に形成された位置に半導体素子101の面の外側に中心部を形成するように形成されている。外部端子部102Bは内部端子部102Aから形成リード部102Cを介して形成され、半導体素子の形成面に形成された位置で半導体素子面に形成する方向に、形成リード102Cが上向きになり、外部端子部102Bはその先に形成し、半導体素子の面に形成する方向で一元的に形成している。即ち、中心部101を形成する2層の外周部102Bの形成を設けている。そして、外部端子部102Bに形成させ、半田（ペースト）からなる外部電極105を形成部105より外部へ突出させて設けている。

1. 絶縁層104としては、100μm程度のポリイミド系の熱可塑性樹脂PM122C（B2化炭素系）

とを用いたが、他には、シリコン系ポリイミド（TA）715（三菱化学株式会社）や硬化型樹脂HCS200（三井化学株式会社）等が用いられる。上記実施例では、半田ペーストからなる外部電極であるが、この部分は半田ペーストに代えてもよい。尚、本発明の製造方法及び装置は、上記のように、パッケージ構造が半導体素子の面側に形成する、面側に形成されたパッケージであるが、形成方向について、10mm以下にすることができ、形成方向に形成するものである。本発明においては外部電極も、半導体素子の端子部（パッド部）に形成された位置に形成し、半導体素子の端子部の位置を二次元的に形成し、内部端子部と外部端子部との一体となった構造を形成し、半導体素子の端子部に二次元的に形成して形成することにより、半導体素子の、一層の多ピン化に十分対応できる。

(0 0 0 9) 次に、本発明のリードフレームの構成を説明し、図にそって説明する。本発明のリードフレームは、上記実施例の半導体素子に形成されたものである。図2は本発明のリードフレームの断面図を示すもので、図2中、200はリードフレーム、201は内部端子部、202は外部端子部、203は形成リード部、204は導電層、205は外部電極である。リードフレームは42合金（Ni42%のFe合金）からなり、リードフレームの厚さは、内部端子部のある厚さで0.05mm、外部端子部のある厚さで0.2mmである。内部端子部の形成する先端部同士を連結する導電部205は厚さ（0.05mm厚）に形成されており、形成する半導体素子を形成する際の打ち込みと金箔にて打ち込みし、形成されている。本発明では外部端子部202は丸状であるが、これに限定されない。また、リードフレーム厚として42合金を用いたがこれに限定されない。銅合金でもよい。

(0 0 1 0) 次に、上記実施例のリードフレームの製造方法を図を用いて簡単に説明する。図4は本発明のリードフレームを製造した工程を示したものである。先ず、42合金（Ni42%のFe合金）からなる、厚さ0.2mmのリードフレーム部材300を準備し、図4(a)は、リードフレーム部材300の両面に形成されたレジスト301を形成し、形成した。（図3(b)）。

次に、リードフレーム部材300の両面から所定のパターンを形成してレジストの所定の部分のみを除去した。即ち、形成し、レジストパターン301Aを形成した。（図3(c)）

尚レジストとしては形成された合金の表面にレジスト（PMERレジスト）を使用した。次に、レジストパターン301Aを形成した。57°C、48時間の硬化後二次硬化を経て、リードフレーム部材300の両面からスプレイングして、形成した。

の基板が図2に示すリードフレームを具備した
(図3(c))。図2(b)のは、図2のA1-A2に
おける基板である。これは、レジストを形成した後、
洗浄処理を施した後、所定の箇所(内部端子部分を含む
領域)のみに金メッキ処理を行った。(図3(e))
尚、上記リードフレームの製造工程においては、図2
(b)に示すように、厚肉部と薄肉部を形成するため、
外部端子形成面からのエッチング(露出)を多く行
い、反対面からは少なめにエッチング(露出)を行っ
た。また、金メッキに加え、銅メッキやパラジウムメ
ッキでも良い。上記のリードフレームの製造方法は、1ヶ
の半導体装置を封入するために必要なリードフレーム1
ヶの製造方法であるが、通常は半導体装置の面から、リード
フレーム部材をエッチング加工する時、図2に示すリ
ードフレームを複数個面付けした状態で作成し、上記の工
程を行う。この場合は、図2に示す外部端子205の一部
に露出する領域(図示していない)をリードフレームの
外側に付けて面付け状態とする。

【0011】次に、上記のようにして作成されたリード
フレームを用いた、本発明の樹脂封入型半導体装置の製
造方法の実施例を図に示して説明する。図4は、本実施
例樹脂封入型半導体装置の製造工程を示すものである。
図3に示すようにして作成されたリードフレーム400
の外部端子部402形成面(図面)と対向する面に、
ポリイミド系熱硬化型の絶縁性材料(テープ)401
(日立化成株式会社製、HM122C)を、400℃
C、6Kg/m²で1.0秒間圧着して貼り付けた(図
4(a))。この状態の平面図を図5に示す。この状態
では、図4(a)の外部端子部402の熱圧着部分(図4(b))、対
向する内部端子部の先端部を露出する露出部403と、
その部分の絶縁性材料(テープ)401とを切り取
った。(図4(c))

次いで、外部端子部402および圧着部406A、40
6Bを用い、外部端子部404を含む不露の部分(図4(d))と同時に、絶縁性材料404を介して半
導体素子407上にリード部408の熱圧着を行った。
(図4(e))

尚、この図4(d)に示す、形成リードと露出してリ
ードフレーム全体を支えている外部端子部204を含む不露の
部分を切り取れば、樹脂封入した状態に付しても良い。こ
の場合には、通常の半導体リードフレームを用いたQFP
パッケージ等のようにダムバー(図示していない)を設
けると良い。リード部410を半導体素子411へ露出
した後、ワイヤ414により、半導体素子の端子(パ
ッド)411Aとリード部410の内部端子410Aと
を電気的に接続した。(図4(f))

その後、所定の金型を用い、エポキシ系の樹脂415で
リード部410の外部端子部410Bのみを固定させ
て、全体を封止した。(図4(g))
ここでは、専用の金型(図示していない)を用いたが、

所定の面(外部端子部)を露し樹脂封入して、必要と
しない面(図4(g)の裏面)は、図4(g)に示す外部
端子部410B上に半導体ペーストをスクリーン印刷によ
り塗布し、半田(ペースト)からなる外部端子部416を
作成し、本発明の樹脂封入型半導体装置を作成した。
(図4(h))

尚、半田からなる外部端子部416の作成は、スクリー
ン印刷に限定されるものではなく、リフローまたはポッテ
イング等でも、図4(g)と半田ペーストとの形成による
半田が得られれば良い。

【0012】

【発明の効果】本発明は、上記のように、更なる樹脂封
入型半導体装置の小型化、高集積化が図られる状態
のもと、半導体装置パッケージサイズにおけるチップの
占有部を上げ、半導体装置の小型化に対応させ、図4(g)
への実装面を露出させる、即ち、図4(g)への実装
面を向上させることが出来る半導体装置の提供を可能と
したものであり、同時に従来のTSSOP等の小型パッ
ケージに図4(g)であった更なる多ピン化を実現した樹脂封入
型半導体装置の提供を可能としたものである。

【図面の簡単な説明】

【図1】本発明の樹脂封入型半導体装置の概略図面図
及び断面図

【図2】本発明のリードフレームの平面図

【図3】本発明のリードフレームの製造工程図

【図4】本発明の樹脂封入型半導体装置の製造工程図

【図5】本発明のリードフレームに絶縁性材料を貼り付
けた状態の平面図

【符号の説明】

100	樹脂封入型半導体装置
101	半導体素子
101A	端子部(パッド部)
102	リード部
102A	内部端子部
102B	外部端子部
102C	形成リード部
103	ワイヤ
104	絶縁性材料
105	樹脂部
106	半田(ペースト)からなる外部
200	リードフレーム
201	内部端子部
202	外部端子部
203	形成リード部
204	露出部
205	外部部
300	リードフレーム部材
301	レジスト

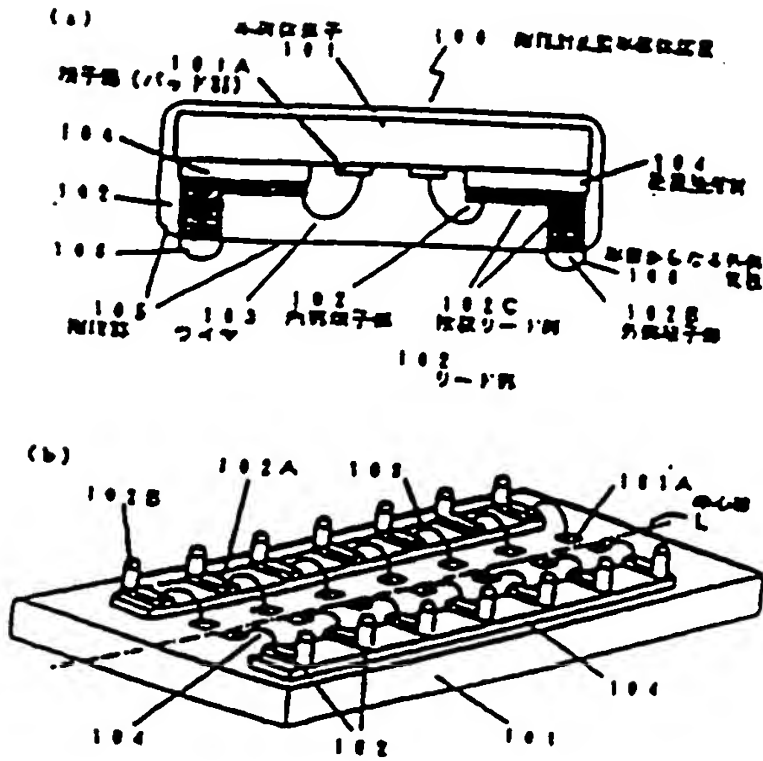
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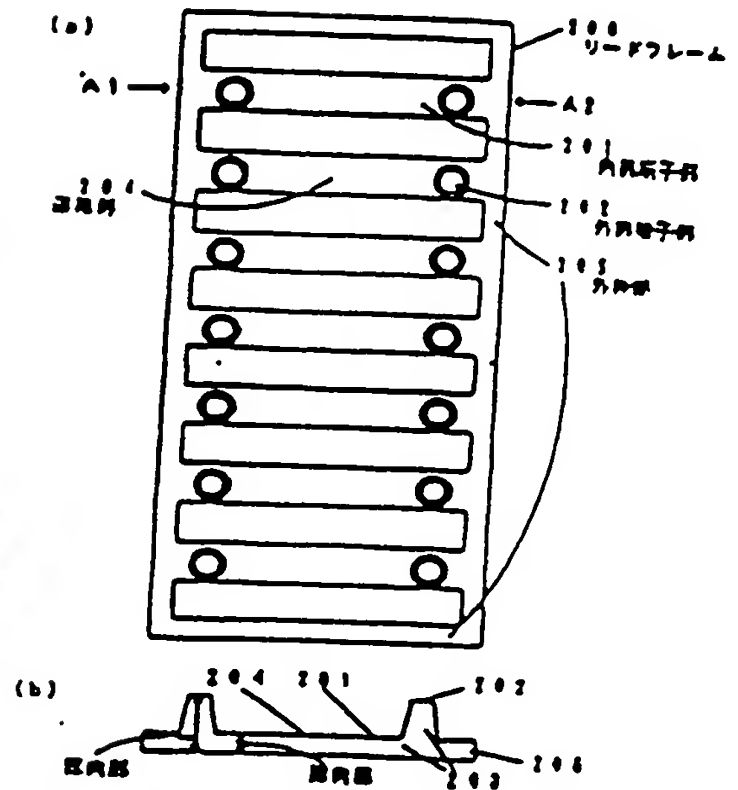
303A 内部端子部
303B 外部端子部
304 送信部
305 受メッキ部
306 外部部
400 リードフレーム
401 絶縁性基材 (テープ)
402 外部端子部
403 送信部

405A, 405E 1750222
406A, 406B 外部1750222および1750222
410 リード部
410A 内部端子部
410B 外部端子部
410C 外部リード部
411 半導体素子
411A ワイヤ
415 基板

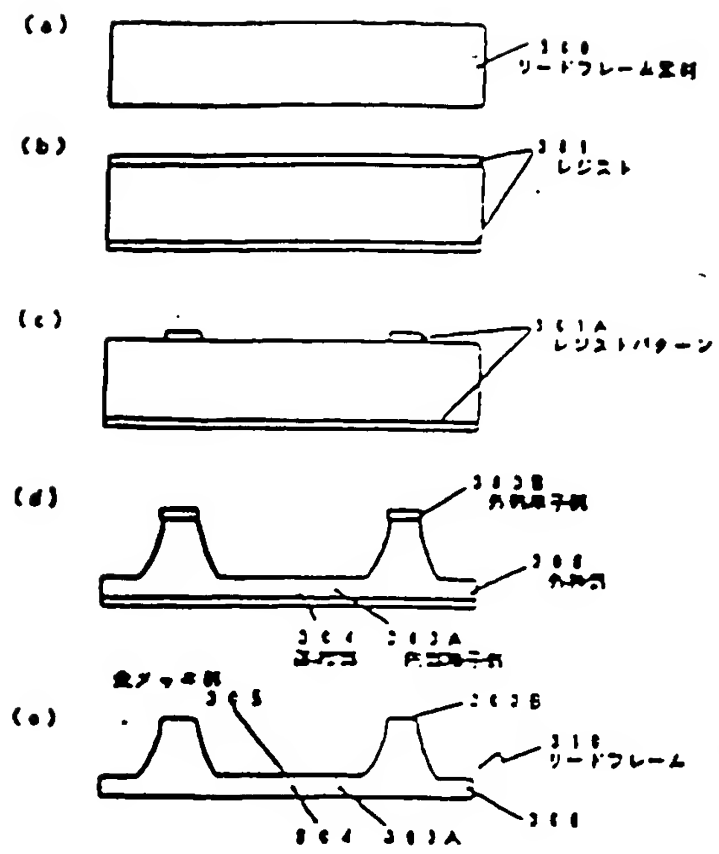
(図 1)



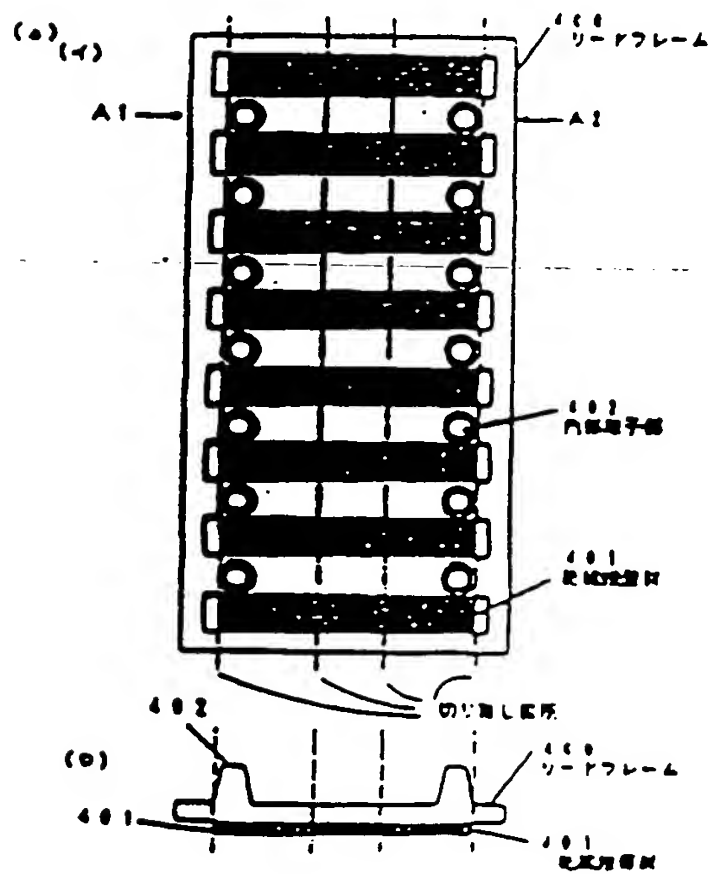
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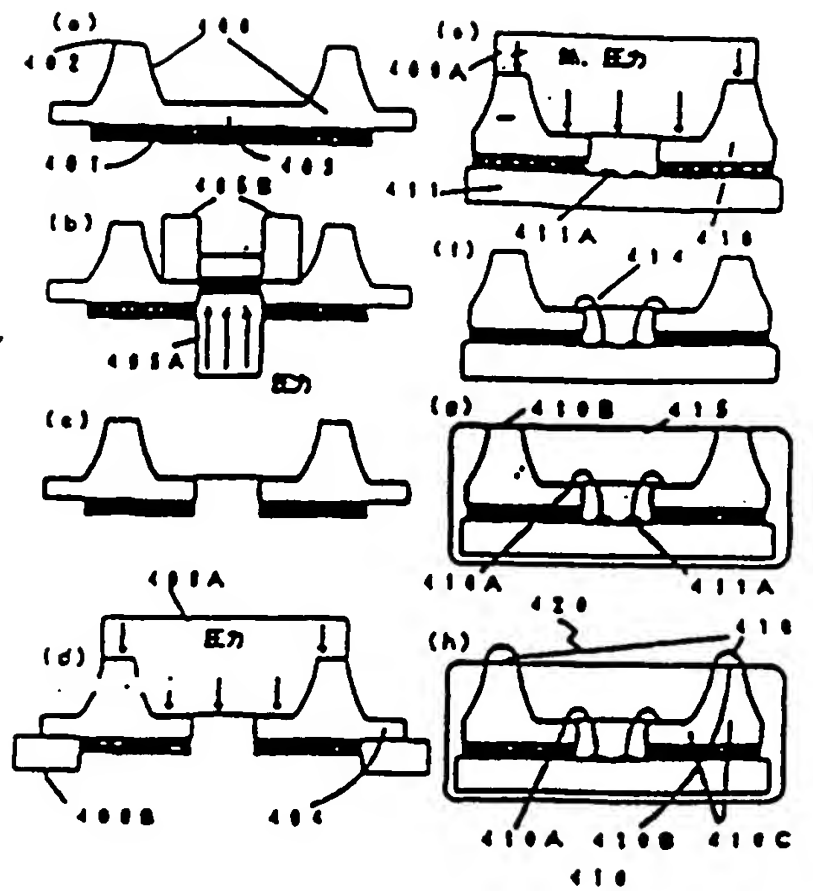
(図 3)



(図 5)



(図 4)



Japanese Patent Laid-Open Publication No. Heisei 8-125066

[TITLE OF THE INVENTION]

Resin Encapsulated Semiconductor Device, Lead Frame
5 Used Therein, and Fabrication Method for the Resin
Encapsulated Semiconductor Device

[CLAIMS]

1. A resin encapsulated semiconductor device
10 comprising:

a semiconductor chip;

a plurality of leads fixedly attached to a terminal-
end surface of the semiconductor chip by an insulating
adhesive interposed between the semiconductor chip and the
15 leads, each of the leads including integral portions, that
is, an inner terminal portion adapted to be electrically
connected to an associated one of terminals of the
semiconductor chip, an outer terminal portion extending
outwardly in a direction orthogonal to the terminal-end
20 surface of the semiconductor chip and adapted to be
connected to an external circuit, and a connecting lead
portion adapted to connect the inner and outer terminal
portions to each other; and

outer electrodes each connected to the outer terminal
25 portion of an associated one of the leads and made of

solder to allow the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate.

5 2. The resin encapsulated semiconductor device according to claim 1, wherein the terminals of the semiconductor chip are arranged along a substantially center line between a pair of sides of the semiconductor chip on the terminal-end surface of the semiconductor chip,
10 and the leads are arranged in two facing sets along the sides of the semiconductor chip, respectively, in such a fashion that the terminals of the semiconductor chip are interposed between the two facing lead sets.

15 3. A lead frame comprising:

a plurality of leads each including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to
20 be connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other;

25 each of the outer terminal portions of the leads being protruded in a direction orthogonal to a lead frame

surface via an associated one of the connecting lead portions;

the inner lead portions of the leads being arranged in pair in such a fashion that the leads of each lead pair have facing tips, respectively;

connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs; and

an outer frame portion arranged outside the outer terminal portions and connected to the connecting lead portions in such a fashion that they form an integral structure together, thereby protecting the entire portion of the lead frame.

4. A method for fabricating a semiconductor device including a semiconductor chip, a plurality of leads fixedly attached to a terminal-end surface of the semiconductor chip by an insulating adhesive-interposed between the semiconductor chip and the leads, each of the leads including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of the semiconductor chip, an outer terminal portion extending outwardly in a direction orthogonal to the terminal-end surface of the semiconductor chip and adapted to be connected to an external circuit,

and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; and outer electrodes each connected to the outer terminal portion of an associated one of the leads and made of solder to allow
5 the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate, comprising the steps of:

(A) fabricating a lead frame including a plurality of leads each including integral portions, that is, an inner
10 terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to be connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and
15 outer terminal portions to each other, each of the outer terminal portions of the leads being protruded in a direction orthogonal to a lead frame surface via an associated one of the connecting lead portions, the inner lead portions of the leads being arranged in pair in such a
20 fashion that the leads of each lead pair have facing tips, respectively, connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs, and an outer frame portion arranged outside the outer terminal portions and connected to the
25 connecting lead portions in such a fashion that they form

an integral structure together, thereby protecting the entire portion of the lead frame;

5 (B) applying an insulating layer to a surface of the lead frame opposite to the outer terminal portions, punching out the connecting portions adapted to connect facing ones of the inner lead portions to each other along with portions of the insulating layer respectively arranged at regions corresponding to the connecting portions by use of punching dies, aligning the punched portions of the lead
10 frame with the terminals of the semiconductor chip, and mounting the entire portion of the lead frame on the semiconductor chip by the adhesive interposed therebetween;

(C) cutting off unnecessary portions of the lead frame including the outer frame portion by use of punching
15 dies, thereby removing the cut-off portions;

(D) wire-bonding the terminals of the semiconductor chip with tips of the inner terminal portions mounted on the semiconductor chip, and encapsulating the semiconductor
chip and the lead frame by a resin while allowing a surface
20 of the lead frame toward the outer terminal portions to be externally exposed; and

(E) forming outer electrodes made of solder on the exposed lead frame surface toward the outer terminal portions.

25

[DETAILED DESCRIPTION OF THE INVENTION]

[FIELD OF THE INVENTION]

The present invention relates to a resin encapsulated semiconductor device (plastic package) in which a semiconductor chip is packaged, and more particularly to a semiconductor device configured to achieve an improvement in mounting density or to have a multi-pinned structure and a method for manufacturing such a semiconductor device.

10 [DESCRIPTION OF THE PRIOR ART]

Recently, semiconductor devices have been developed to have a higher integration degree and a higher performance by virtue of developments of techniques associated with an increase in integration degree and miniaturization and in pace with the tendency of electronic appliances to have a high performance and a light, thin, simple, and miniature structure. A representative example of such semiconductor devices is an ASIC of LSI. For instance, developments of resin encapsulated semiconductor device plastic packages have been advanced from surface-mounting packages such as SOJs (Small Outlined-Leaded Packages) or QFPs (Quad Flat Packages) to packages having a miniature structure mainly achieved in accordance with a thinness obtained by virtue of developments of TSOPs (Tin Small Outline Packages) or to LOC (Lead On Chip) structures

adapted to achieve an improvement in the chip packaging efficiency by virtue of developments of an internal three-dimensional package structure. In addition to an increase in integration degree and improvement in performance, there has also been growing demand for an increase in the number of pins, thickness, and miniaturization of resin encapsulated semiconductor packages. In the above mentioned conventional packages, however, there is a limitation in miniaturization because those packages have a structure in which leads are arranged around a chip. Similarly, leads are arranged around a chip in the case of miniature packages such as TSOPs. In such packages, there is also a limitation in increasing the number of pins due to the pin pitch used.

[SUBJECT MATTERS TO BE SOLVED BY THE INVENTION]

As mentioned above, there has been demand for an increase in integration degree and improvement in performance of resin encapsulated semiconductor devices. Also, there has also been growing demand for an increase in the number of pins, thickness, and miniaturization of resin encapsulated semiconductor packages. In such situations, the present invention makes it possible to increase the occupancy degree of a chip in a semiconductor package with a limited size while reducing the mounting area of the

semiconductor package on a circuit board to achieve a miniaturization of the resulting semiconductor device. That is, the present invention is adapted to provide a resin encapsulated semiconductor device capable of achieving an improvement in the mounting density thereof on a circuit board. Also, the present invention is adapted to achieve an increase in the number of pins which is difficult in miniature packages such as conventional TSOPs.

10 [MEANS FOR SOLVING THE SUBJECT MATTERS]

The resin encapsulated semiconductor device of the present invention is characterized in that it comprises: a semiconductor chip; a plurality of leads fixedly attached to a terminal-end surface of the semiconductor chip by an insulating adhesive interposed between the semiconductor chip and the leads, each of the leads including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of the semiconductor chip, an outer terminal portion extending outwardly in a direction orthogonal to the terminal-end surface of the semiconductor chip and adapted to be connected to an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; and outer electrodes each connected to the outer terminal portion of an associated one of the

leads and made of solder to allow the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate. The above semiconductor device can be embodied into a BGA (Ball Grid Array) type resin encapsulated semiconductor device by arranging a plurality of leads each having an inner terminal portion and an outer terminal portion integral with each other in a two-dimensional fashion on the terminal-end surface of the semiconductor chip and forming the outer electrodes in the form of solder balls.

The above semiconductor device is also characterized in that the terminals of the semiconductor chip are arranged along a substantially center line between a pair of sides of the semiconductor chip on the terminal-end surface of the semiconductor chip, and the leads are arranged in two facing sets along the sides of the semiconductor chip, respectively, in such a fashion that the terminals of the semiconductor chip are interposed between the two facing lead sets. The lead frame of the present invention is characterized in that it comprises: a plurality of leads each including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to be

connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; each of the outer terminal portions of the leads being protruded in a direction orthogonal to a lead frame surface via an associated one of the connecting lead portions; the inner lead portions of the leads being arranged in pair in such a fashion that the leads of each lead pair have facing tips, respectively; connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs; and an outer frame portion arranged outside the outer terminal portions and connected to the connecting lead portions in such a fashion that they form an integral structure together, thereby protecting the entire portion of the lead frame. The above lead frame can be embodied into a lead frame for a BGA (Ball Grid Array) type resin encapsulated semiconductor device by arranging a plurality of leads each having an inner terminal portion and an outer terminal portion integral with each other in a two-dimensional fashion on the terminal-end surface of the semiconductor chip and forming the outer electrodes in the form of solder balls.

The present invention is also characterized by a method for fabricating a semiconductor device including a semiconductor chip, a plurality of leads fixedly attached

to a terminal-end surface of the semiconductor chip by an insulating adhesive interposed between the semiconductor chip and the leads, each of the leads including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of the semiconductor chip, an outer terminal portion extending outwardly in a direction orthogonal to the terminal-end surface of the semiconductor chip and adapted to be connected to an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other; and outer electrodes each connected to the outer terminal portion of an associated one of the leads and made of solder to allow the semiconductor device to be mounted on a circuit board, at least a part of the outer leads being externally exposed from a resin encapsulate, comprising the steps of: (A) fabricating a lead frame including a plurality of leads each including integral portions, that is, an inner terminal portion adapted to be electrically connected to an associated one of terminals of a semiconductor chip, an outer terminal portion adapted to be connected to an associated one of terminals of an external circuit, and a connecting lead portion adapted to connect the inner and outer terminal portions to each other, each of the outer terminal portions of the leads being protruded in a direction orthogonal to a

lead frame surface via an associated one of the connecting lead portions, the inner lead portions of the leads being arranged in pair in such a fashion that the leads of each lead pair have facing tips, respectively, connecting portions each adapted to connect the facing tips of the leads included in an associated one of the lead pairs, and an outer frame portion arranged outside the outer terminal portions and connected to the connecting lead portions in such a fashion that they form an integral structure together, thereby protecting the entire portion of the lead frame; (B) applying an insulating layer to a surface of the lead frame opposite to the outer terminal portions, punching out the connecting portions adapted to connect facing ones of the inner lead portions to each other along with portions of the insulating layer respectively arranged at regions corresponding to the connecting portions by use of punching dies, aligning the punched portions of the lead frame with the terminals of the semiconductor chip, and mounting the entire portion of the lead frame on the semiconductor chip by the adhesive interposed therebetween; (C) cutting off unnecessary portions of the lead frame including the outer frame portion by use of punching dies, thereby removing the cut-off portions; (D) wire-bonding the terminals of the semiconductor chip with tips of the inner terminal portions mounted on the semiconductor chip, and

encapsulating the semiconductor chip and the lead frame by
a resin while allowing a surface of the lead frame toward
the outer terminal portions to be externally exposed; and
(E) forming outer electrodes made of solder on the exposed
5 lead frame surface toward the outer terminal portions.

[FUNCTIONS]

With the above mentioned configuration, the resin
encapsulated semiconductor device of the present invention
10 can increase the occupancy degree of the chip while
achieving a miniaturization thereof. That is, the resin
encapsulated semiconductor device is capable of reducing
the mounting area thereof on a circuit board and achieving
an improvement in the mounting density thereof on the
15 circuit board. In particular, the present invention
achieves a miniaturization of the semiconductor device by
fixedly attaching a plurality of leads each including an
inner terminal portion and an outer terminal portion
integral with each other to a surface of a semiconductor
20 chip by an insulating adhesive layer interposed between the
semiconductor chip and the leads, and connecting outer
electrodes made of solder to the outer terminal portions,
respectively. Also, the present invention achieves an
increase in the number of pins in the semiconductor device
25 by arranging the outer electrodes made of solder in a two-

dimensional fashion on a plane parallel to the surface of the semiconductor chip. Where the outer electrodes made of solder are formed in the form of solder balls and arranged in a two-dimensional fashion, a BGA type semiconductor device capable of achieving an increase in the number of pins can be obtained. In the above semiconductor device, the terminals of the semiconductor chip are arranged along a substantially center line between a pair of sides of the semiconductor chip on the terminal-end surface of the semiconductor chip, and the leads are arranged in two facing sets along the sides of the semiconductor chip, respectively, in such a fashion that the terminals of the semiconductor chip are interposed between the two facing lead sets. Thus, the semiconductor device has a simple structure suitable in regard to productivity. The lead frame of the present invention makes it possible to fabricate the above mentioned resin encapsulated semiconductor device by virtue of there above mentioned configuration thereof. However, this lead frame can be fabricated using a half etching method during an etching process as used for conventional lead frames. The method for fabricating a resin encapsulated semiconductor device in accordance with the present invention involves the steps of applying an insulating layer to a surface of the lead frame opposite to the outer terminal portions, punching out

the connecting portions adapted to connect facing ones of the inner lead portions to each other along with portions of the insulating layer respectively arranged at regions corresponding to the connecting portions by use of punching dies, aligning the punched portions of the lead frame with the terminals of the semiconductor chip, and mounting the entire portion of the lead frame on the semiconductor chip by the adhesive interposed therebetween, and cutting off unnecessary portions of the lead frame including the outer frame portion by use of punching dies, thereby removing the cut-off portions. Thus, a plurality of leads each including an inner terminal portion and an outer terminal portion integral with each other are mounted on a semiconductor chip. Accordingly, the present invention makes it possible to achieve a miniaturization of semiconductor devices. In accordance with the present invention, it is also possible to fabricate a resin encapsulated semiconductor device having an increased number of pins.

20

[EMBODIMENTS]

Hereinafter, embodiments of the present invention associated with resin encapsulated semiconductor devices will be described in conjunction with the annexed drawings. Fig. 1A is a cross-sectional view schematically

25

illustrating a resin encapsulated semiconductor device according to an embodiment of the present invention. Fig. 1B is a perspective view illustrating an essential part of the resin encapsulated semiconductor device. Figs. 1A and 1B, the reference numeral 100 denotes the resin encapsulated semiconductor device, 101 a semiconductor chip, 102 leads, 102A inner terminal portions, 102B outer terminal portions, 102C connecting lead portions, 101A contacts (pads), 103 wires, 104 an insulating adhesive, 105 a resin encapsulate, 106 outer electrodes made of solder (paste), respectively. The resin encapsulated semiconductor device according to this embodiment is fabricated using a lead frame which will be described hereinafter. In this resin encapsulated semiconductor device, a plurality of L-shaped leads 102, each of which has an inner terminal portion 102A and an outer terminal portion 102 integral with each other, are mounted on a semiconductor chip 101 by means of an insulating adhesive 104. An outer electrode 106, which is made of solder, is attached to each outer terminal portion 102B. The outer electrode 106 is outwardly protruded from a resin encapsulate 105. The resin encapsulated semiconductor device configured as mentioned above has a package area substantially equal to the entire area thereof. When this semiconductor device is mounted on a circuit board, the

solder is melted and then solidified to allow the outer terminal portions 102B to be electrically connected to an external circuit. In the resin encapsulated semiconductor device according to the illustrated embodiment, contacts (pads) 101A provided at the semiconductor chip 101 are arranged in pairs along a center line L of the semiconductor chip 101 at opposite sides of the center line L in such a fashion that contacts included in each contact pair face each other. The outer terminal portion 102B of each lead is spaced apart from the inner terminal portion 102A of the lead. Between the inner and outer terminal portions 102A and 102B, a connecting lead portion 102C is interposed. The connecting lead portion 102C of each lead is bent in a direction orthogonal to the major surface of the semiconductor chip at a position near an associated one of the side surfaces of the semiconductor chip 101, so that it has an L shape. In each lead, the outer terminal portion 102B is arranged at an end of the connecting lead portion 102C. The outer terminal portions 102B of the leads are arranged in a one-dimensional fashion on a plane parallel to the major surface of the semiconductor chip 101. That is, the outer terminal portions 102B are arranged in two lines at opposite sides of the center line L. As mentioned above, one outer electrode 106 made of solder is connected to the outer terminal portion 102B of

each lead and outwardly exposed from the resin encapsulate
105.

For the insulating adhesive 104, a polyimide-based thermoplastic adhesive having a thickness of 100 μm (HM122C manufactured by Hitachi Chemical Co., Ltd.) is preferably
5 used. Alternatively, a silicon denaturalized polyimide adhesive (ITA1715 manufactured by Sumitomo Bakelite Co., Ltd.) or a thermosetting adhesive (HG5200 manufactured by Tomoekawa Papermaking Co., Ltd.) may be used. Although
10 outer electrodes made of solder paste are used in the illustrated embodiment, solder balls may be used.

As mentioned above, the resin encapsulated semiconductor device according to the illustrated embodiment has a package area substantially equal to the
15 entire area thereof. That is, the illustrated embodiment of the present invention provides a package having a compact structure in regard to area. In accordance with the present invention, a thinned package structure can also be provided in that it is also possible to reduce the
20 package thickness to about 1.0 mm or less. Although the outer electrodes have been described as being arranged in two lines along the contacts (pads) of the semiconductor chip, they may be arranged in a two-dimensional fashion. This is achieved by arranging contacts of the semiconductor
25 chip in a two-dimensional fashion. On the surface of the

semiconductor chip arranged with those contacts, a plurality of terminal sets each having an inner terminal and outer terminal integral with each other are arranged in a two-dimensional fashion. In this case, it is possible to
5 fabricate a semiconductor device using a semiconductor chip with an increased number of pins.

An embodiment of the present invention associated with a lead frame will now be described. The lead frame according to this embodiment is adapted to be used in the
10 above mentioned semiconductor device. Fig. 2 is a plan view of the lead frame according to this embodiment. In Fig. 2, the reference numeral 200 denotes a lead frame, 201 inner terminal portions, 202 outer terminal portions, 203 connecting lead portions, 204 a connecting portion, and 205
15 an outer frame portion, respectively. The lead frame is made of 42 ALLOY (namely, an Fe alloy containing 42% Ni). The lead frame has a thickness of 0.05 mm at its thinner portion, that is, the inner terminal portions, and a thickness of 0.2 mm at its thicker portion, that is, the
20 outer terminal portions. The connecting portion, which connects facing tips of the inner terminal portions to each other, has a thickness of 0.05 mm corresponding to that of the thinner portion. This connecting portion has a structure capable of allowing an easy punching thereof in
25 the fabrication of the semiconductor device, as described

hereinafter. Although the outer terminal portions 202 have a ball shape in the illustrated embodiment, they are not limited to this shape. Also, although the lead frame has been described as being made of the 42 ALLOY, it is not limited to this material. For the lead frame, a copper-based alloy may be used.

Now, fabrication of the lead frame according to the illustrated embodiment will be described in brief. Fig. 4 illustrates a process for fabricating the lead frame according to the illustrated embodiment. First, a lead frame blank 300 having a thickness of 0.2 mm was prepared which is made of a 42 ALLOY (an Fe alloy containing 42% Ni). The prepared lead frame blank 300 was then subjected to a cleaning process, thereby removing grease from the surfaces thereof (Fig. 3a). Subsequently, photoresist films 301 were coated over both surfaces of the lead frame blank 300, respectively. The coated photoresist films 301 were then dried (Fig. 3b).

Using desired pattern plates, the photoresist films 301 on both surfaces of the lead frame blank 300 were exposed to light at their desired portions. A developing process was then conducted to the light-exposed photoresist films 301, thereby forming photoresist patterns 301A.

For the photoresist films, a negative liquid-phase resist (PMER resist) manufactured by Tokyo Ohka Co., Ltd.

was used. Using the resist patterns 301A as anti-etch films, the lead frame blank 300 was subjected to a spray etching process at both surfaces thereof. The spray etching process was conducted using a ferric chloride solution of 48 BAUME at 57 °C. Thus, a lead frame having a structure of Fig. 2a was obtained (Fig. 3d). Fig. 2a is a plan view of the lead frame. Fig. 2b is a cross-sectional view taken along the line A1 - A2 of Fig. 2a. Thereafter, the remaining photoresist thin films were peeled off. The resulting structure was then subjected to a cleaning process. A gold plating process was subsequently conducted for desired portions of the lead frame, that is, regions including inner terminal portions (Fig. 3e).

In the fabrication process of the lead frame, the etching process was conducted with a large etch depth at one major surface of the lead frame blank where outer terminal portions are to be formed, and with a small etch depth at the other major surface of the lead frame. In place of the gold plating, silver or palladium plating may be utilized. The above mentioned lead frame fabrication process is adapted to manufacture a single lead frame required for the manufacture of a single semiconductor device. In terms of productivity, however, the etching process is conducted for lead frame units each corresponding to the single lead frame shown in Fig. 2. To

this end, a frame member (not shown) is provided at a desired portion of the peripheral edge of the lead frame so as to connect a desired part of the outer frame portion 205 shown in Fig. 2 to a corresponding one of an adjacent lead
5 frame.

Using the lead frame fabricated as mentioned above, the resin encapsulated semiconductor device according to the present invention was fabricated. Now, a method for fabricating the resin encapsulated semiconductor device in
10 accordance with an embodiment of the present invention will be described. Fig. 4 illustrates the method for fabricating the resin encapsulated semiconductor device in accordance with the embodiment of the present invention. A polyimide-based thermosetting insulating adhesive (tape)
15 401 (HM122C manufactured by Hitachi Chemical Co., Ltd.) was applied to one surface, formed with the outer terminal portions 402, of the lead frame 400 fabricated as in Fig. 3 and the outer surface of the lead frame 400 using a hot pressing process conducted at 400 °C and 6 Kg/m² for 1.0
20 second Fig. 4a). The resulting structure is shown in Fig. 5 which is a plan view. Thereafter, the connecting portions 403 connecting facing tips of the inner terminal portions were punched using punching dies 405A and 405B (Fig. 4b). Also, portions of the insulating adhesive

(tape) corresponding to those connecting portions 403 were punched (Fig. 4c).

Subsequently, unnecessary portions of the lead frame including the outer frame 404 were cut off using outer frame punching and pressing dies 406A and 406B (Fig. 4d).
5 The lead frame was then bonded to a semiconductor chip 407 at its leads 410 under pressure while applying heat (Fig. 4e).

The process for cutting off the unnecessary portion of the lead frame including the outer frame 404 supporting
10 the entire portion of the lead frame along with the connecting lead portion, as shown in Fig. 4d, may be carried out after an resin encapsulating process. In this case, dam bars (not shown) are preferably provided, as in
15 QFP packages typically using a lead frame having a single layer structure. After the mounting of the leads 410 on the semiconductor chip 411, the inner terminal portion 410 of each lead 410 was electrically connected to an
associated one of terminals (pads) 411A of the
20 semiconductor chip 411 (Fig. 4f).

Subsequently, an epoxy-based resin 415 was molded to encapsulate the resulting structure while exposing the outer terminal portions 410B of the leads 410 using a desired mold (Fig. 4g).

Although a specific mold (not shown) was used for the above process in the illustrated case, use of such a die may be unnecessary in so far as the resin encapsulating process can be conducted under the condition in which
5 desired portions (outer terminal portions) of the lead frame are left. Thereafter, a solder paste was coated on the exposed outer terminal portions 410B in accordance with a screen printing process, thereby forming outer electrodes
10 416 made of solder (paste). Thus, the fabrication of the resin encapsulated semiconductor device according to the present invention was achieved (Fig. 4h).

Although the formation of the outer electrodes 416 made of solder has been described as being achieved using a screen printing process, it may be achieved using a reflow
15 or bonding process in so far as an amount of solder required for a connection of the semiconductor device to a circuit board is obtained.

(EFFECTS OF THE INVENTION)

20 As apparent from the above description, the present invention makes it possible to increase the occupancy degree of a semiconductor chip in a semiconductor package in situations requiring new resin encapsulated
25 semiconductor devices having a highly integrated structure while exhibiting a high performance. The present invention

also makes it possible to reduce the area of the semiconductor device on a circuit board in order to cope with a compactness of the semiconductor device. That is, the present invention can provide a semiconductor device
5 capable of achieving an improvement in the mounting density on a circuit board. At the same time, the present invention can provide a resin encapsulated semiconductor device having a new multipinned structure which could not be realized in compact packages such as conventional TSOPs.